Please amend the claims as follows:

1. (Once amended) A method for developing fully functional transparent memory modules using [chip] independent memory parts, comprising the steps of:

testing the parts for failed segments;

sorting the parts according to the results of the testing;

identifying failed and working segments in [the] selected parts; and

combining the working segments [amongst] of different selected memory parts, including working segments of at least one partially defective memory part [parts, in an effective manner to create an effective] to form a fully functional transparent memory module.

3. (Once amended) The method of claim 1, wherein at least one of the memory parts is a package.

4. (Once amended) The method of claim 1, further comprising;

testing the completed memory module as to its operational status to approve the module for use or to identify any operating problems; and , as required, changing the combination of working segments of memory parts to overcome any such identified problem [wherein at least one of the parts must be replaced by a substitute part].

5.(once amended) A memory module formed [made] by the method of claim 4 [, wherein the memory module is made up of repaired and the substituted parts].

6. (once amended) The method of claim 1, wherein the combination of working segments is done by patching using solder-dot connections [to provide a logical oring of sets of I/O lines] on a printed circuit board.

8. (Once amended) A method for developing effective chip-on-board memory modules, using a selected combination of independent partially defective memory parts and good memory parts, comprising the steps of:

assembling the selected parts as primary parts and backup parts onto a chip-on-board memory module assembly;

testing the module for failed I/O lines in the parts;

identifying the operating segments in the parts, including operating segments in at least one of the partially defective memory parts; and

combining the working segments of a partially defective primary part with required working segments of backup parts [an effective manner to create] to form an effective fully functional transparent memory module.

12. (Once amended) A process for patching primary memory parts with [partially defective] backup memory parts to form [create] a memory module functionally [transparant] transparent to the user, comprising the steps of:

testing the primary memory parts and the [partially defective] backup memory parts before mounting the parts on a board;

identify operating and failed segments of the primary parts and of the [partially defective] backup memory parts;

determining which operating I/O lines from the [partially defective] backup memory parts to use for patching the failed segments of the primary parts; and

substituting said determined operating I/O lines from the backup parts for failed lines in the failed segments of one or more primary parts [part components] to form a [resultant] completed memory module.

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15. (Once amended)The method of claim 12, further comprising;

testing the completed memory module as to its operational status to approve the module for use or to identify any operating problems; and, as required,

the step of replacing at least one of the parts with a replacement part to overcome any such identified operating problem.

16. (Once amended) A memory module made by the ~~process~~ method of claim 15, wherein the memory module comprises all good, [repaired] partially defective, and [the] replacement parts.

17. (Once amended) The method of claim 12, wherein the patching is done by using solder-dot connections [to provide a logical oring of sets of I/O lines] on a printed circuit board.

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24. (Once amended) A memory module made by the ~~process~~ method of claim 19, wherein the memory module comprises all good, partially defective and [the] replacement parts.

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31. (Once amended) [A module made by the process] The module of claim 27, wherein the module comprises all good, partially defective and [the] replacement parts.

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50. (Once amended) A process for selecting primary parts and [partially defective] backup parts on a chip-on-board module assembly, comprising the steps of:

performing a wafer test on a memory die;

selecting [a combination of] as primary parts, dies that have a reasonable probability of being patched successfully;

selecting backup parts for assembly on a PC module;

assembling the selected primary and backup parts on the PC module;

applying a plastic [overcoating] over coating to the assembled parts; and
test the module using a chip test applied at the module pins.

51. (Once amended) The process of claim 50, further comprising the steps of:
assigning a bar code to the module to identify failed bits;
fill in the solder-dot locations of the primary parts, the solder-dot locations of the back-up parts are left open;
test the module on a full function circuit tester, wherein failed bits are noted, and the module is assigned a bar-code identifying the failed bits;
generate patching instruction charts for the module, wherein the development of the patching instruction charts includes an optimization pass designed to maximize use of smaller patch parts, leaving the larger parts [avaliable] available for patching later-discovered failures;
disconnect solder-dot connections [ont] on the primary parts to isolate [the] any failed line;
fill the solder-dot connections to patch in [the substitite] substitute lines, the solder-dot connections selected as identified in the patching instruction charts;
re-test the module, including high temperature stress testing of the module.

53. (Once amended) A memory module made up of primary parts and partially defective backup parts, comprising:
at least four primary parts, the primary parts having at least one line failure, and the primary parts are [layed] laid out horizontally with a card edge;
at least four partially defective parts;
a module PC board containing a pattern of solder-dot connections, the solder-dot connections allowing any failing primary part I/O lines to be replaced by I/O substitute lines from the backup parts;
wherein the failing line is disconnected from the primary part by removing the solder of its solder dot connection and the substitute line is connected by filling the applicable solder-dot, the replacement line having the equivalent function as the failing line so that the module is transparent to the user.

56. (Once amended) The memory module of claim 53, wherein at least one of the primary parts is an extended [a extedned] data out part that runs at about 60 nsec.

60. (Once amended) The memory module of claim 53, further comprising a variable voltage regulator, the variable voltage regulator connected to the module PC board, wherein the variable voltage regulator works with the extended data out primary part by tying [tieing] output enable to ground.

61. (Once amended) The memory module of claim 53, further comprising a variable voltage regulator, the variable voltage regulator connected to the module PC board, wherein the variable voltage

regulator works with the Fast Page primary part by tying [tieing] output enable to ground.

65. (Once amended) [Any method for testing] Testing of the die level to decide the packaging type and the mixture of parts to be used on a memory module for optimum utilization, comprising the steps of; test a wafer; identify the working and [nonworking] non-working segments in the parts; optimize utilization of working segments using decision tables to decide optimum packaging or combination of devices on a module.

Please add the following claims:

66. A memory module comprising:
primary part memory means for storing data;
independent backup part memory means for storing data;
connection means for selectively substituting an operational I/O data line of said backup memory means for a failed I/O data line of said primary memory means.

67. A memory module in accordance with claim 66 wherein:
said memory module has a target memory capacity X,
said primary part memory means has a memory capacity X minus the capacity of any defective I/O data lines therein; and
said independent backup part memory means has available memory capacity at least equal to the capacity of said defective I/O data lines.

68. A memory module in accordance with claim 66 wherein:
said connection means comprises a pattern of solder dot connections.

69. A memory module in accordance with claim 66 wherein:
said connection means comprises a pattern of jumper wire connections.

70. A memory module in accordance with claim 66 wherein:
said primary part memory means comprise 1MX16 parts; and
said backup part memory means comprise 1MX4 parts.

71. A method for constructing a fully functional memory module which utilizes partially defective independent memory circuit parts comprising:
(a) testing and classifying memory parts in a set of defined classifications
(b) selecting a primary memory part having a selected classification;
(c) selecting a backup memory part having a selected different classification; and
(d) constructing a memory module wherein: any defective data lines of the selected primary memory part are replaced by operational data lines of the backup circuit structure.

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